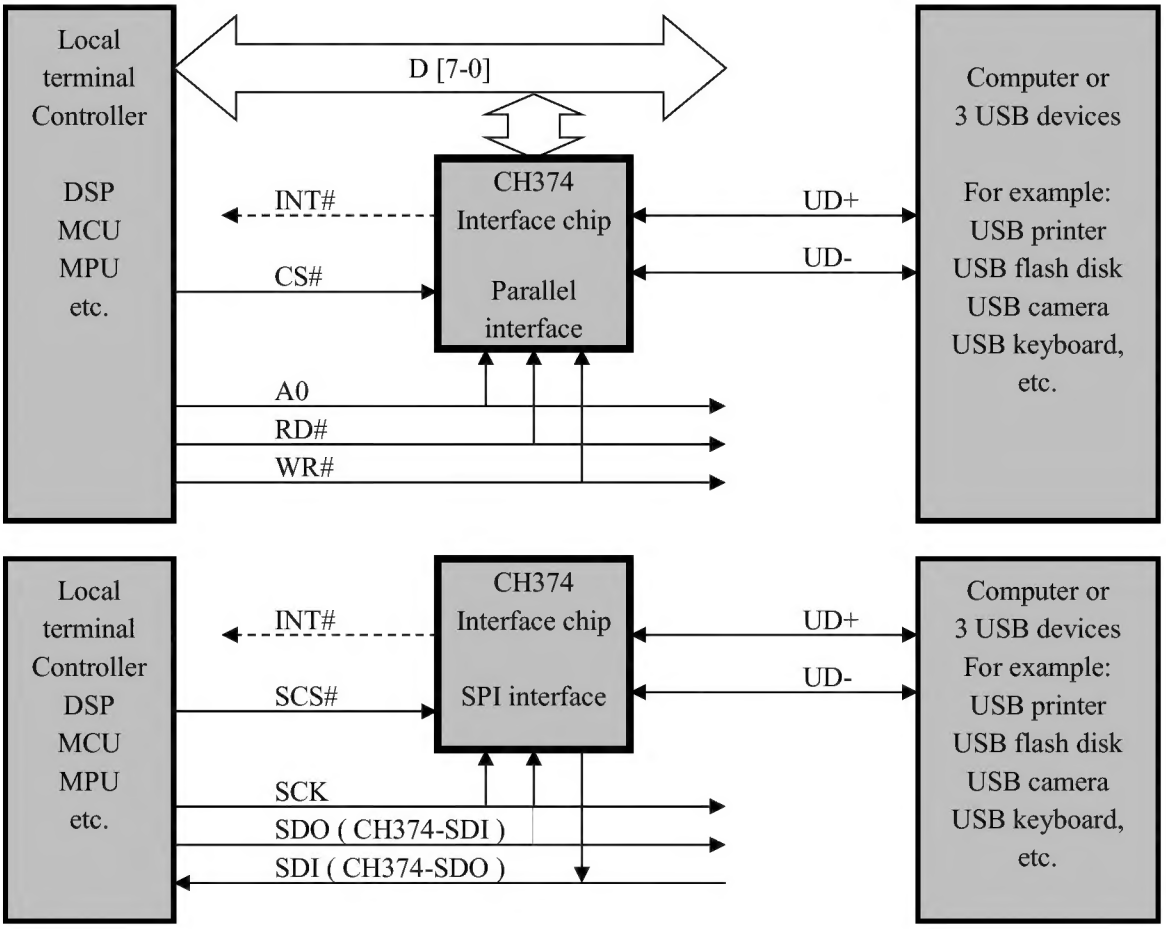
USB Bus Interface Chip CH374

Datasheet
Version: 3B
http://wch.cn

1. Overview

CH374 is a universal interface chip for USB bus, supports USB-HOST mode and USB-DEVICE/SLAVE mode, has 3-port root HUB, supports low-speed and full-speed control transmission, bulk transmission, interrupt transmission and synchronous/isochronous transmission. At the local side, CH374 has an8-bit data bus, a read, write and chip selection control line and an interrupt output, and can be easily hooked to the system bus of DSP/MCU/MPU and other controllers. In addition, CH374 also provides SPI serial communication mode saving I/O pins, being connected with DSP/MCU/MPU through 3-line or 4-line SPI serial interface and interrupt output.

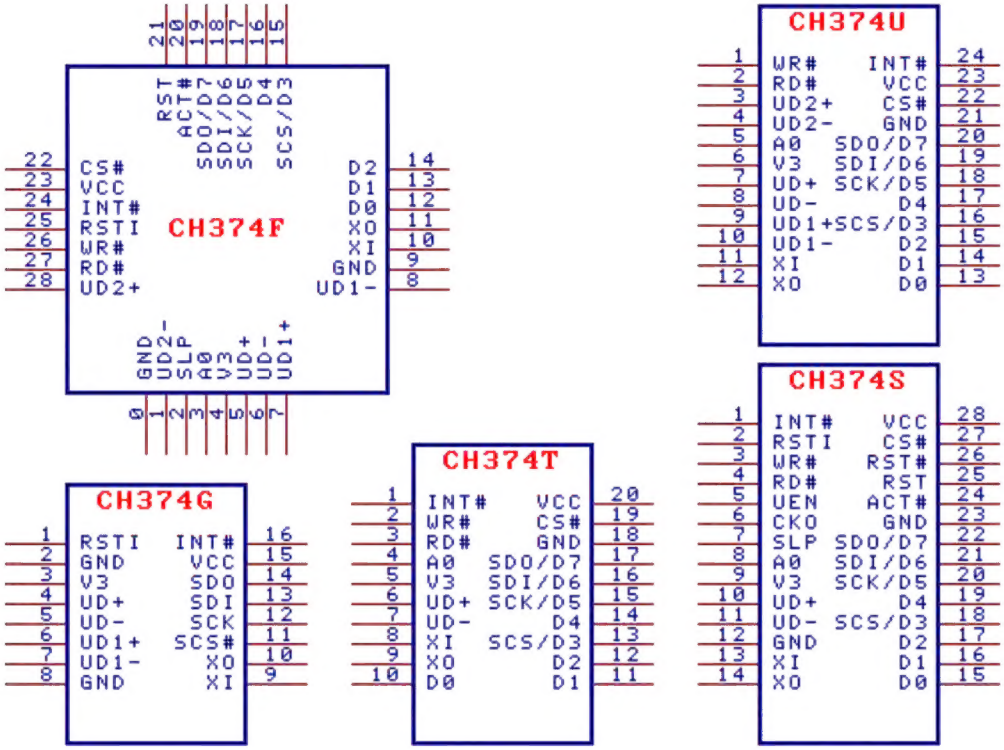


2. Features

- Support 1.5Mbps low-speed and 12Mbps full-speed USB communication, compatible with USB V2.0; only capacitors are required for peripheral components.
- Support USB-HOST interface and USB-Device interface, and support dynamic mode switching between HOST and DEVICE.
- CH374F/U chip has 3-port USB ROOT-HUB, and can connect and manage 3 USB devices simultaneously.
- Support commonly used low-speed and full-speed USB device control transmission, bulk transmission, interrupt transmission and synchronous/isochronous transmission.

- Automatically detect the low-speed and full-speed connection and disconnection of USB device, and provide interrupt notifications for device connection and disconnection.
- The USB signal line impedance matching series resistance, pull-up resistor at the USB device terminal and pull-down resistor at the USB host terminal are provided internally.
- Two MCU interfaces are optional: 6MB 8-bit passive parallel interface and 3.5MB/28MHz SPI serial interface.
- The parallel interface contains an 8-bit data bus, a 1-bit address, and a 3-wire control: chip selection input, write strobe and optional read strobe.
- The parallel interface only occupies two address bits: index address port and data port. The internal index address automatically increases after the data port is read and written.
- The SPI serial interface includes SPI chip selection, serial clock, serial input and output, and SPI output and input can be connected in parallel.
- The interrupt output pin is an optional connection and is active at low level. It can be replaced by querying the interrupt flag bit in the register.
- Provide miscellaneous function: programmable clock output, power on reset output and optional watchdog reset.
- Provide USB flash disk file level subroutine library supporting FAT12/FAT16/FAT32 file system, achieving USB flash disk file read and write by MCU.
- Support supply voltages of 5V, 3.3V and 3V.
- Provide QFN-28, SSOP-24, SOP-16, SOP-28 and SSOP-20 lead-free package, be compatible with RoHS, provide DIP28 conversion board, and pins are basically compatible with CH375 and CH372.

3. Package



Package	Width of Plastic		Pitch of Pin		Instruction of Package	Ordering Information
QFN28_4X4	4*4mm		0.4mm	15.7mil	Square leadless 28-pin	CH374F

SSOP-24	5.30mm	209mil	0.65mm	25mil	Subminiature 24-pin patch	CH374U
SOP-16	3.9mm	150mil	1.27mm	50mil	Standard 16-pin patch	CH374G
SOP-28	7.62mm	300mil	1.27mm	50mil	Standard 28-pin patch	CH374S
SSOP-20	5.30mm	209mil	0.65mm	25mil	Subminiature 20-pin patch	CH374T

Notes: 1. Only CH374F can be externally connected to a crystal and a capacitor, or use the built-in clock directly without external connection;
Other CH374 chips do not support the built-in clock, and crystals and oscillation capacitors must be externally connected.
2. For new designs, please give priority to CH374F, CH374U and CH374G.

4. Pins

374F Pin No.	374U Pin No.	374G Pin No.	374S Pin No.	374T Pin No.	Pin Name	Pin Type	Pin description
23	23	15	28	20	VCC	Power	A 0.1uF power decoupling capacitor is required to be connected externally to the positive power input terminal.
9, 0 bottom PAD	21	2, 8	12, 23	18	GND	Power	Common ground, required to be connected to the ground wire of the USB bus
4	6	3	9	5	V3	Power	Connected to the VCC input external power at the supply voltage of 3.3V The external capacity is 0.1uF decoupling capacitor at 5V supply voltage
10	11	9	13	8	XI	Input	The input terminal of the crystal oscillator shall be externally connected to a crystal and an oscillating capacitor. For the internal clock mode of CH374F, XI shall be connected to GND.
11	12	10	14	9	XO	Output	The inverted output terminal of the crystal oscillator shall be externally connected to a crystal and an oscillating capacitor. For the internal clock mode of CH374F, XO shall be suspended.
5	7	4	10	6	UD+	USB signal	USB bus D + data cable, USB bus root hub HUB0 D + data cable
6	8	5	11	7	UD-	USB signal	USB bus D - data cable, USB bus root hub HUB0 D - data cable
7	9	6	None	None	UD1+	USB signal	USB bus root hub HUB1 D + data cable
8	10	7	None	None	UD1-	USB signal	USB bus root hub HUB1 D - data cable
28	3	None	None	None	UD2+	USB signal	USB bus root hub HUB2 D + data cable

1	4	None	None	None	UD2-	USB signal	USB bus root hub HUB2 D - data cable
19～12	20～13	11, 12, 13, 14	22～15	17～10	D7～D0	Bilateral Three-state	8-bit bidirectional data bus, built-in weak pull-up resistor D3 is also SCS# of SPI interface, D5 is also SCK of SPI interface, D6 is also SDI of SPI interface, D7 is also SDO of SPI interface
27	2	None	4	3	RD#	Input	Reading strobe input, active at low level, built-in weak pull-up resistor
26	1	None	3	2	WR#	Input	Writing strobe input, active at low level, built-in weak pull-up resistor
22	22	None	27	19	CS#	Input	Chip selection control input, active at low level, built-in weak pull-up resistor
24	24	16	1	1	INT#	Open-drain Output	Interrupt request output, active at low level, built-in pull-up resistor
3	5	None	8	4	A0	Input	Address wire input, index port and data port distinguished, built-in weak pull-up resistor; when A0 is 1, write the index address; when A0 is 0, read and write data
20	None	None	24	None	ACT#	Open-drain Output	USB transmission/active state output in USB device mode, USB device connection status output in USB host mode, Active at low level, built-in pull-up resistor
None	None	None	5	None	UEN	Input	USB signal UD+/UD- output enable, built-in pull-down resistor
None	None	None	6	None	CKO	Output	Programmable clock output, It must be suspended when not in use, and the connection shall be shortened as much as possible
25	None	1	2	None	RSTI	Input	External reset input, active at high level, built-in pull-down resistor
21	None	None	25	None	RST	Output	Power-on rest output and external reset output, active at high level
None	None	None	26	None	RST#	Output	Power-on rest output and external reset output, active at low level
2	None	None	7	None	SLP	Output	Sleep state output, active at high level

5. Registers

MCU referred to in this manual is basically applicable to DSP or SCM/MCU/MPU/CPU, etc.

The internal register and buffer area of CH374 are allocated in the address range from 00H to 0FFH, and are accessed after being addressed by MCU.

The default value after reset is expressed in binary number, and its characteristics can be described by several character flags, which are as follows:

0: Always 0 after reset;

1: Always 1 after reset;

X: This bit is automatically set by internal hardware or affected by the status of external pins;

=: Reset does not affect the data, and the initial value of the data is uncertain;

?: Reserved bit; the read data has no meaning. You must write 0 or keep the original value when writing.

Address range Hexadecimal system	Register name (marked in gray) Bit name of register	Register description (marked in gray) Bit description of the register	Default value after software and hardware reset
00H	Reserved	Disable reading and writing	????????
01H	REG_SYS_AUX	System auxiliary setting register (Note: only CH374F, CH374U and CH374G with batch No. of 2017XXXXX support this register)	00000010
Bits 7-4 of 01H	Reserved	The data read is meaningless and must be 0000	0000/????
Bit 3 of 01H	BIT_GP_BIT	Universal bit variable, which can defining the software	0
Bit 2 of 01H	BIT_EP0_16BYTES	Endpoint 0 supports a maximum 16-byte data length mode: 0 = maximum 8-byte mode, endpoint 0 transceiver buffer is independent; 1 = maximum 16-byte mode, endpoint 0 transceiver buffer is shared	0
Bit 1 of 01H Bit 0 of 01H	Reversal of hardware identification bit	Fixed value, always constant 10, Used to verify that the hardware connection is correct and the reading operation is successful	10
02H	REG_HUB_SETUP	ROOT-HUB configuration register in host mode	10XXX000
Bit 7 of 02H	BIT_HUB_DISABLE	ROOT-HUB functions: 0 = Allowed (in USB host mode only), 1 = Disabled	1
Bit 6 of 02H	BIT_HUB_PRE_PID	Low-speed prefix packet PRE PID output control: 0 = Disabled, 1 = Allowed (the external device is USB-HUB)	0
Bit 5 of 02H	BIT_HUB2_DX_IN	Sampling status of UD2+ at HUB2 full speed/UD2- at low speed: 0=low level/speed mismatch, 1=high level/speed match	X
Bit 4 of 02H	BIT_HUB1_DX_IN	Sampling status of UD1+ at HUB1 full speed/UD1- at low speed: 0=low level/speed mismatch, 1=high level/speed match	X
Bit 3 of 02H	BIT_HUB0_ATTACH	USB device connection status of HUB0 port: 0 = not connected/disconnected/unplugged, 1 = connected/plugged	X
Bit 2 of 02H	BIT_HUB0_POLAR	Signal polarity control of HUB0 port: 0 = positive polarity/full speed, 1 = negative polarity/low speed	0

Bit 1 of 02H	BIT_HUB0_RESET	USB bus reset control of HUB0 port: 0 = no reset; 1 = USB bus reset	0
Bit 0 of 02H	BIT_HUB0_EN	USB transmission enable of HUB0 port: 0 = Disable USB transmission, 1 = Allow USB transmission	0
03H	REG_HUB_CTRL	ROOT-HUB control register in USB host mode	X000X000
Bit 7 of 03H	BIT_HUB2_ATTACH	USB device connection status of HUB2 port: 0 = not connected/disconnected/unplugged, 1 = connected/plugged	X
Bit 6 of 03H	BIT_HUB2_POLAR	Signal polarity control of HUB2 port: 0 = positive polarity/full speed, 1 = negative polarity/low speed	0
Bit 5 of 03H	BIT_HUB2_RESET	USB bus reset control of HUB2 port: 0 = no reset; 1 = USB bus reset	0
Bit 4 of 03H	BIT_HUB2_EN	USB transmission enable of HUB2 port: 0 = Disable USB transmission, 1 = Allow USB transmission	0
Bit 3 of 03H	BIT_HUB1_ATTACH	USB device connection status of HUB1 port: 0 = not connected/disconnected/unplugged, 1 = connected/plugged	X
Bit 2 of 03H	BIT_HUB1_POLAR	Signal polarity control of HUB1 port: 0 = positive polarity/full speed, 1 = negative polarity/low speed	0
Bit 1 of 03H	BIT_HUB1_RESET	USB bus reset control of HUB1 port: 0 = no reset; 1 = USB bus reset	0
Bit 0 of 03H	BIT_HUB1_EN	USB transmission enable of HUB1 port: 0 = Disable USB transmission, 1 = Allow USB transmission	0
04H	REG_SYS_INFO	System information register, only reading	XXX?XX01
Bit 7 of 04H	BIT_INFO_POWER_RST	Completion status of hardware power-on reset: 0=resetting; 1=reset completed	0/X
Bit 6 of 04H	BIT_INFO_WAKE_UP	The chip wake-up status is not affected by software reset: 0=sleeping or waking up; 1=waken up	X
Bit 5 of 04H	BIT_INFO_SOF_PRES	Hardware 1mS timing cycle status, 1 =SOF packet will be generated in host mode	=/X
Bit 4 of 04H	BIT_INFO_CLK_8KHZ	Hardware 8KHz clock bit	X
Bit 3 of 04H	BIT_INFO_USB_DP	Logic level state of USB bus UD+ pin	X
Bit 2 of 04H	BIT_INFO_USB_DM	Logic level state of USB bus UD- pin	X
Bit 1 of 04H Bit 0 of 04H	Hardware identification bit	Fixed value, always constant 01, Used to verify that the hardware connection is correct and the reading operation is successful	01
05H	REG_SYS_CTRL	System control register, not affected by the software reset	00000000

Bit 7 of 05H	Power to Set Aside	The data read is meaningless and must be 0	0/?
Bit 1 of 05H	(Before enabling ROOT-HUB) BIT_CTRL_OE_POLAR	When BIT_HUB_DISABLE = 1, USB output enable polarity of UEN pin: 0 = high level enable, and UD+/- output is disabled if UEN is low; 1 = low level enable, and UD+/- output is disabled if UEN is high;	0
Bit 1 of 05H	(After enabling ROOT-HUB) Power to Set Aside	When BIT_HUB_DISABLE = 0, the data read is meaningless and must be 1, equivalently, BIT_CTRL_OE_POLAR bit must be set to 1	0
Bit 5 of 05H	BIT_CTRL_INT_PULSE	Interrupt output mode of INT# pin: 0 = Low level interrupt, until the corresponding interrupt flag is cleared; 1 = Low level pulse interrupt	0
Bit 4 of 05H	BIT_CTRL_WATCH_DOG	Watchdog reset enable of RST pin and RST# pin: 0= Disabled, only power on reset, no watchdog reset; 1= Enabled, cannot be disabled once enabled, unless the hardware is reset	0
Bit 3 of 05H	BIT_CTRL_RESET_NOW	Chip software reset control: 0=no reset; 1=reset	0
Bit 2 of 05H	BIT_CTRL_USB_POWER	USB power source regulator control of V3 pin: 0=Enabled, generating USB power from 5V power source of VCC pin; 1= Disabled; the USB power source can be externally inputted from the V3 pin	0
Bit 1 of 05H	BIT_CTRL_CLK_12MHZ	Selection of XI pin input clock frequency: 0=24MHz；1=12MHz	0
Bit 0 of 05H	BIT_CTRL_OSCIL_OFF	Clock oscillator control: 0=oscillation allowed; 1=oscillation stopped	0
06H	REG_USB_SETUP	USB configuration register	00000000
Bit 7 of 06H	BIT_SETP_HOST_MODE	USB master-slave mode: 0 = device mode; 1 = host mode	0
Bit 6 of 06H	BIT_SETP_LED_ACT	Low level activation event of ACT# pin in device mode: 0 = Transceiving transmission process; 1 = USB host active	0
Bit 6 of 06H	BIT_SETP_AUTO_SOF	Automatically generate SOF packet enable in host mode: 0=Disabled; 1=Enabled, sending out SOF packet automatically	0
Bit 5 of 06H Bit 4 of 06H	(Before enabling ROOT-HUB) BIT_SETP_USB_SPEED	USB bus rate when BIT_HUB_DISABLE = 1: 00=12Mbps in full speed mode; 11=1.5Mbps in low speed mode; Other value = disabled	00

Bit 5 of 06H	(After enabling ROOT-HUB) BIT_SETP_LOW_SPEED	USB bus transmission speed when BIT_HUB_DISABLE = 0: 0=12Mbps；1=1.5Mbps	0
Bit 4 of 06H	(After enabling ROOT-HUB) Reserved	When BIT_HUB_DISABLE = 0, The data read is meaningless and must be 0	0/?
Bit 3 of 06H Bit 2 of 06H	BIT_SETP_RAM_MODE	Backup buffer area application method: 00 = Disable the backup buffer; 01= Connect the receive buffer to continuously receive 128 bytes, The start address is RAM_ENDP2_EXCH/RAM_HOST_EXCH; 10=the second buffer area of continuous sending, the synchronization flag 1 selected; 11=the second buffer area of continuous receiving, the synchronization flag 1 selected;	00
Bit 1 of 06H	BIT_SETP_PULLUP_EN	USB pull-up resistor control in device mode: 0 = Disable the pull-up resistor; 1 = Enable the pull-up resistor/connection	0
Bit 0 of 06H	BIT_SETP_TRANS_EN	USB device transmission enable in device mode: 0 = Disabled, 1 = Allowed, enable USB device/allow transceiving	0
Bit 1 of 06H Bit 0 of 06H	(Before enabling ROOT-HUB) BIT_SETP_BUS_CTRL Reserved after enabling ROOT-HUB	When BIT_HUB_DISABLE = 1, USB bus status control in host mode: 00=normal/idle; 01=UD+low UD-low (bus reset); 10=disabled; 11=UD+low UD-high (bus recovery)	00
Bit 1 of 06H Bit 0 of 06H	(After enabling ROOT-HUB) Reserved	When BIT_HUB_DISABLE = 0, The data read is meaningless and must be 0	00/??
07H	REG_INTER_EN	Interrupt enable register, including programmable clock settings	11110000
Bits 7-4 of 07H	BIT_IE_CLK_OUT_DIV	Frequency division divisor of programmable clock: Output frequency = (48MHz/(this value + 1)), Example: 0001 = 24 MHz; 0010 = 16 MHz; 1111=3MHz	1111
Bit 3 of 07H	BIT_IE_USB_RESUME	USB bus resume/wake-up interrupt enable: 0 = Enable chip wake-up completion interrupt BIT_IF_WAKE_UP; 1 = Enable USB bus resume interrupt BIT_IF_USB_RESUME	0
Bit 2 of 07H	BIT_IE_USB_SUSPEND	USB bus suspend interrupt enable: 0=disabled; 1=enabled, output from INT# pin	0
Bit 1 of 07H	BIT_IE_BUS_RESET	USB bus reset interrupt enable in device mode:	0

		0=disabled; 1=enabled, output from INT# pin	
Bit 1 of 07H	BIT_IE_DEV_DETECT	USB device detection interrupt enable in host mode: 0=disabled; 1=enabled, output from INT# pin	0
Bit 0 of 07H	BIT_IE_TRANSFER	USB transmission completion interrupt enable: 0=disabled; 1=enabled, output from INT# pin	0
08H	REG_USB_ADDR	USB device address register	00000000
Bit 7 of 08H	Reserved	The data read is meaningless and must be 0	0/?
Bits 6-0 of 08H	BIT_ADDR_USB_DEV	Address of USB device in device mode, Address of USB device currently operated in host mode: ;	0000000
09H	REG_INTER_FLAG	Interrupt flag register, only reading	XXX00000
Bit 7 of 09H	BIT_IF_USB_DX_IN	Sampling status of UD+ at HUB0 full speed/UD- at low speed: 0=low level/speed mismatch; 1=high level/speed match	X
Bit 6 of 09H	BIT_IF_USB_OE	USB output enable status input from UEN pin: 0 = UEN pin is at low level; 1 = UEN pin is at high level	X
Bit 5 of 09H	BIT_IF_DEV_ATTACH	Current connection status of USB device: 0= no USB device is connected/disconnected/unplugged; 1= at least one USB device has been connected/plugged in	=/X
Bit 4 of 09H	BIT_IF_USB_PAUSE	USB transmission pause flag, Effective in case of 1; writing 1 to this bit to clear the flag, This bit is automatically set to 1 after each USB transfer is completed	0/X
Bit 3 of 09H	BIT_IF_WAKE_UP	Chip wake-up completion interrupt flag, Effective in case of 1; writing 1 to this bit to clear the flag, This bit is automatically set to 1 after the chip wake-up is completed	0/X
Bit 3 of 09H	BIT_IF_USB_RESUME	USB bus resume/wake-up interrupt flag, Effective in case of 1; writing 1 to this bit to clear the flag, This bit is automatically set to 1 after detecting that the USB device is resumed	0/X
Bit 2 of 09H	BIT_IF_USB_SUSPEND	USB bus suspend interrupt flag, Effective in case of 1; writing 1 to this bit to clear the flag, This bit is automatically set to 1 after detecting that the USB device is suspended	0/X
Bit 1 of 09H	BIT_IF_BUS_RESET	USB bus reset interrupt flag in device mode, Effective in case of 1; writing 1 to this bit to clear the flag,	0/X

		This bit is automatically set to 1 after detecting that the USB device is reset	
Bit 1 of 09H	BIT_IF_DEV_DETECT	USB device plug detection interrupt enable in host mode, Effective in case of 1; writing 1 to this bit to clear the flag, This bit is automatically set to 1 after detecting that the USB device is plugged or unplugged	0/X
Bit 0 of 09H	BIT_IF_TRANSFER	USB transmission completion interrupt flag, Effective in case of 1; writing 1 to this bit to clear the flag, This bit is automatically set to 1 after each USB transfer is completed	0/X
0AH	REG_USB_STATUS	USB status register, reading only, Usually only querying after the corresponding interrupt is detected	1XXXXXXX
Bit 7 of 0AH	BIT_STAT_SIE_FREE	Status of current USB interface engine SIE: 0=busy/transmitting; 1=idle/waiting	1/X
Bit 6 of 0AH	BIT_STAT_SUSPEND	Current USB bus suspended status: 0 = Bus active; 1 = Bus suspended	X
Bit 5 of 0AH	BIT_STAT_BUS_RESET	Current USB bus reset status in device mode: 0 = USB bus idle/normal/no reset; 1 = USB bus being reset	X
Bit 4 of 0AH	BIT_STAT_TOG_MATCH	Indicating whether the current USB transmission is successful: 0= transmission failure; 1= transmission success and synchronization	X
Bit 3 of 0AH Bit 2 of 0AH	BIT_STAT_THIS_PID	Token PID of USB transmission transaction in device mode: 00 = OUT transaction; 01 = Reserved/accident; 10 = IN transaction; 11 = SETUP transaction	XX
Bit 1 of 0AH Bit 0 of 0AH	BIT_STAT_THIS_ENDP	Destination endpoint number of USB transmission transaction in device mode: 00 = Endpoint 0; 01 = Endpoint 1; 10 = Endpoint 2; 11 = Reserved/accident	XX
Bits 3-0 of 0AH	BIT_STAT_DEV_RESP	Response PID of USB device in host mode: 0010= transaction reply ACK of device for OUT/SETUP; 1010= transaction reply NAK of device for IN/OUT/SETUP; 1110= transaction reply STALL of device for IN/OUT/SETUP; 0011= transaction reply DATA0 of device for IN 1011= transaction reply DATA1 of device for IN XX00=device reply error or no reply in case	XXXX

		of timeout; Other values = illegal response/accident	
0BH	REG_USB_LENGTH	USB length register, reading only/writing only, Read the receiving length of the current USB transmission, Write the sending length of USB endpoint 2 in device mode, Write the sending length of the USB host in the host mode	XXXXXXXX
0CH	REG_USB_ENDP0	USB endpoint 0 control register in device mode	00000000
Bit 7 of 0CH	BIT_EP0_RECV_TOG	Endpoint 0 receiving synchronization flag: 0 = DATA0; 1 = DATA1	0
Bit 6 of 0CH	BIT_EP0_TRAN_TOG	Endpoint 0 sending synchronization flag: 0 = DATA0; 1 = DATA1	0
Bit 5 of 0CH Bit 4 of 0CH	BIT_EP0_RECV_RESP	Endpoint 0 receiving response (to an OUT transaction): 00 = Response ACK; 01 = Disabled; 10 = Response NAK; 11 = Response STALL	00
Bits 3-0 of 0CH	BIT_EP0_TRAN_RESP	Endpoint 0 sending response (to an IN transaction): 0000 to 1000 = response data length 0 to 8; 1110 = Response NAK; 1111 = Response STALL; Other value = disabled	0000
0DH	REG_USB_ENDP1	USB endpoint 1 control register in device mode	========
Bit 7 of 0DH	BIT_EP1_RECV_TOG	Endpoint 1 receiving synchronization flag: 0 = DATA0; 1 = DATA1	=
Bit 6 of 0DH	BIT_EP1_TRAN_TOG	Endpoint 1 sending synchronization flag: 0 = DATA0; 1 = DATA1	=
Bit 5 of 0DH Bit 4 of 0DH	BIT_EP1_RECV_RESP	Endpoint 1 receiving response (to an OUT transaction): 00 = Response ACK; 01 = Disabled; 10 = Response NAK; 11 = Response STALL	=
Bits 3-0 of 0DH	BIT_EP1_TRAN_RESP	Endpoint 1 sending response (to an IN transaction): 0000 to 1000 = response data length 0 to 8; 1110 = Response NAK; 1111 = Response STALL; Other value = disabled	====
0EH	REG_USB_ENDP2	USB endpoint 2 control register in device mode	00000000
Bit 7 of 0EH	BIT_EP2_RECV_TOG	Endpoint 2 receiving synchronization flag: 0 = DATA0; 1 = DATA1	0
Bit 6 of 0EH	BIT_EP2_TRAN_TOG	Endpoint 2 sending synchronization flag: 0 = DATA0; 1 = DATA1	0
Bit 5 of	BIT_EP2_RECV_RESP	Endpoint 2 receiving response (to an OUT	00

0EH Bit 4 of 0EH		transaction): 00 = Response ACK; 01 = Synchronous/isochronous transmission; 10 = Response NAK; 11 = Response STALL	
Bit 3 of 0EH	Reserved	The data read is meaningless and must be 0	0/?
Bit 2 of 0EH	Reserved	The data read is meaningless and must be 0	0/?
Bit 1 of 0EH Bit 0 of 0EH	BIT_EP2_TRAN_RESP	Endpoint 2 sending response (to an IN transaction): 00 = Response DATA0/DATA1; 01 = Synchronous/isochronous transmission; 10 = Response NAK; 11 = Response STALL	00
0DH	REG_USB_H_TOKEN	USB host token register in host mode	========
Bits 7-4 of 0DH	BIT_HOST_PID_TOKEN	Specify transaction/token PID: 1101=SETUP transaction; 0001=OUT transaction; 1001=IN transaction; 0101=SOF packet; other values=disabled. Note: After the SOF packet is completed, there is no interrupt, and SIE status can be queried	====
Bits 3-0 of 0DH	BIT_HOST_PID_ENDP	Specify the number of destination terminal to be operated: 0000 to 1111=terminal number 0 to 15	====
0EH	REG_USB_H_CTRL	USB host control register in host mode	00000000
Bit 7 of 0EH	BIT_HOST_RECV_TOG	Host receiving synchronization flag: 0=DATA0; 1=DATA1	0
Bit 6 of 0EH	BIT_HOST_TRAN_TOG	Host sending synchronization flag: 0=DATA0; 1=DATA1	0
Bit 5 of 0EH	Reserved	The data read is meaningless and must be 0	0/?
Bit 4 of 0EH	BIT_HOST_RECV_ISO	Type of transmission received by the host: 0 = Control/bulk/interrupt transmission; 1 = Synchronous/isochronous transmission	0
Bit 3 of 0EH	BIT_HOST_START	Host transmission start control: 0=pause; 1=transmission enabled, automatically cleared to 0 after completion	0
Bit 2 of 0EH	Reserved	The data read is meaningless and must be 0	0/?
Bit 1 of 0EH	Reserved	The data read is meaningless and must be 0	0/?
Bit 0 of 0EH	BIT_HOST_TRAN_ISO	Type of transmission sent by the host: 0 = Control/bulk/interrupt transmission; 1 = Synchronous/isochronous transmission	0
0FH-1FH	Reserved	Disable reading and writing	????????
20H-27H	RAM_ENDP0_TRAN	Endpoint 0 send buffer in USB device mode	========
28H-2FH	RAM_ENDP0_RECV	(BIT_EP0_16BYTES=0) in 8-byte mode, Endpoint 0 receive buffer in USB device mode	========
20H-2FH	RAM_ENDP0_BUF	(BIT_EP0_16BYTES=1) in 16-byte mode,	========

		Endpoint 0 receive and send buffers in USB device mode	
30H-37H	RAM_ENDP1_TRAN	Endpoint 1 send buffer in USB device mode	========
38H-3FH	RAM_ENDP1_RECV	Endpoint 1 receive buffer in USB device mode	========
40H-7FH	RAM_ENDP2_TRAN	Endpoint 2 send buffer in USB device mode	========
C0H-FFH	RAM_ENDP2_RECV	Endpoint 2 receive buffer in USB device mode	========
80H-BFH	RAM_ENDP2_EXCH	Endpoint 2 spare buffer in USB device mode	========
40H-7FH	RAM_HOST_TRAN	Send buffer in USB host mode	========
C0H-FFH	RAM_HOST_RECV	Receive buffer in USB host mode	========
80H-BFH	RAM_HOST_EXCH	Standby buffer in USB host mode	========

6. Function Specification

6.1. MCU Interfaces

CH374 provides a universal 8-bit passive parallel interface at the local terminal and SPI synchronous serial interface (CH374G only supports SPI interface mode). During the power on reset of CH374, CH374 will sample the status of CS#, WR# and RD# pins. If both WR# and RD# are at low level (grounded) and CS# is at the high (connected to the positive power source), select the SPI serial interface. Otherwise, select the parallel interface.

The interrupt request of INT# pin output of CH374 is active at low level by default and can be connected to the interrupt input pin or ordinary input pin of MCU. MCU can get the interrupt request of CH374 in interrupt mode or query mode. To save pins, MCU can directly query the interrupt flag register REG_INTER_FLAG of CH374 to learn the interrupt without being connected to the INT# pin of CH374.

6.2. Parallel Interfaces

The parallel port signal line includes: 8-bit bidirectional data lines D7-D0, read strobe input pin RD#, write strobe input pin WR#, chip selection input pin CS# and address input pin A0. Through the passive parallel interface, CH374 can be easily hooked to the system bus of 8-bit DSP or MCU, and can coexist with a number of peripheral devices.

CS# of CH374 is driven by the address decoding circuit, and can be used for device selection when MCU has multiple peripheral devices.

For MCU similiar to the Intel parallel port timing sequence, RD# and WR# pins of CH374 can be connected to the read strobe output pin and write strobe output pin of MCU respectively. For MCU similar to Motorola parallel port time sequence, the RD# pin of the CH374 shall be connected to the low level, and the WR# pin shall be connected to the reading and writing direction output pin R/-W of MCU.

The following table is the truth table of the parallel port I/O operation (X in the table means that this bit is not concerned, and Z means that three states of CH374 are disabled).

CS#	WR#	RD#	A0	D7-D0	Actual operation on CH374
1	0	0	X	X/Z	Sampling is started for selecting SPI port mode during the power-on reset of CH374
1	X	X	X	X/Z	CH374 is not selected, and no any operation is made
0	1	1	X	X/Z	Although selected, no any operation is made
0	0	1/X	1	Input	Write the index address to CH374, which is the starting address for subsequent reading and writing operations
0	0	1/X	0	Input	Write data to the specified address, and the index address will increase progressively after completion, facilitating continuous reading and writing
0	1	0	0	Output	Read data from the specified address. The index address will increase progressively after completion, facilitating the continuous reading and

					writing
0	1	0	1	Output	Read data from the specified address. The index address is unchanged, not applicable to address 20H or above, only for registers within the address range of 00H-1FH, easy to write back after reading and modifying

CH374 occupies two address bits. When the A0 pin is high, select the index address port, and you can write a new index address, or read data but keep the index address unchanged; select the data port when the A0 pin is at the low level. You can read and write the data corresponding to the index address, and automatically add 1 to the index address after the reading and writing operation is completed to facilitate the continuous reading and writing of the next data. The steps for MCU to read and write to CH374 through an 8-bit parallel port are: Firstly, write the index address from the index address port, and then read and write several data continuously.

The auto increment of index address is only applicable to the buffer areas with address no less than 20H, and not applicable to registers with address less than 20H.

6.3. Serial Peripheral Interface, SPI

The SPI synchronous serial interface signal lines include: SPI chip selection input pin SCS#, serial clock input pin SCK, serial data input pin SDI and serial data output pin SDO. CH374 can be hooked to SPI serial buses of various DSP and MCU with fewer connections through SPI serial interface by using less connecting wires, or be connected point-to-point over a longer distance.

SCS# pin of CH374 is driven by the SPI chip selection output pin or the general output pin of MCU. SCK pin is driven by the SPI clock output pin SCK of MCU. SDI pin is driven by the SPI data output pin SDO or MOSI, and SDO pin is connected to the SPI data input pin SDI or MISO of MCU. For the hardware SPI interface, it is recommended that the SPI setting is CPOL=CPHA=0 or CPOL=CPHA=1, and the data bit sequence is MSB first.

The SPI interface of CH374 supports MCU to simulate SPI interface for communication with the common I/O pins. SDO of CH374 is a three-state output pin, which will only output after receiving a read operation command. To save pins, SDO pin of CH374 can be connected in parallel with SDI pin and then connected to the bidirectional I/O pin of MCU. It is recommended that SDO pin of CH374 shall be connected with a resistor with resistance of a few hundred ohms in series and then connected to SDI pin in parallel.

The SPI interface of CH374 supports SPI mode 0 and SPI mode 3. CH374 always inputs data from the rising edge of the SPI clock SCK, and outputs data from the falling edge of SCK when the output is allowed. The data bit sequence is MSB first, and 8 full bits are a byte.

Operation procedure of SPI:

① MCU generates the SPI chip selection of CH374, which is active at low level;

② MCU sends out a one-byte address code according to the SPI output mode, which is used to specify the initial address of subsequent reading and writing operations;

③ MCU sends out a one-byte command code to indicate the operation direction. The reading operation command code is C0H, and the writing operation command code is 80H;

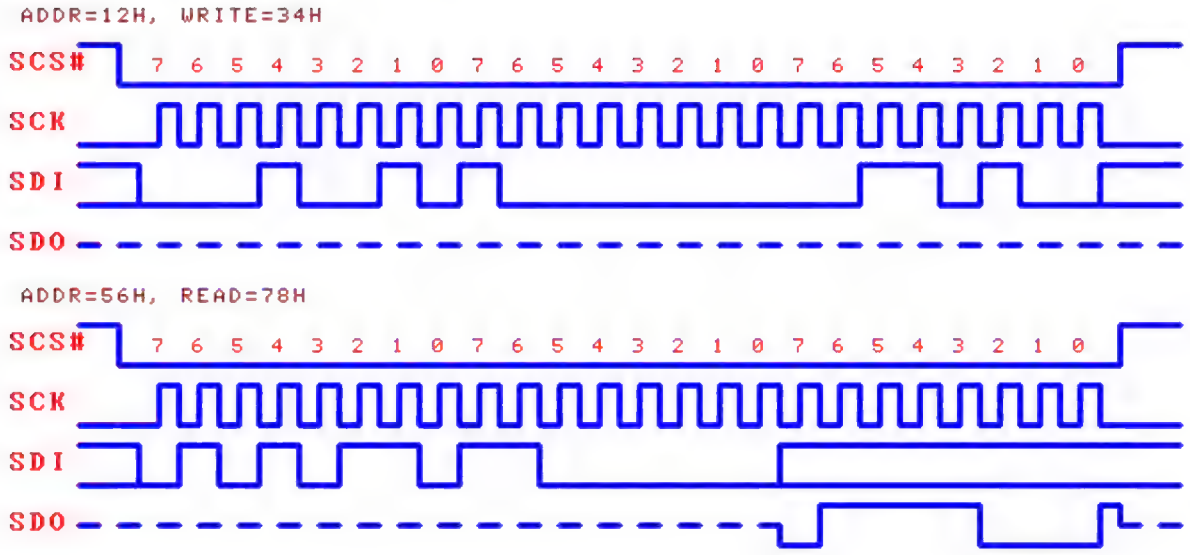
④ For the writing operation, MCU sends out one-byte data to be written, and CH374 receives and saves it to the specified address, and then, the address is automatically increased by 1. The MCU continues to send several bytes of data to be written, and CH374 processes them in sequence until the MCU disables the SPI chip selection;

⑤ For the reading operation, CH374 reads one-byte data from the designated address and the address is automatically increased by 1 after output. MCU receives and saves the data. CH374 continuously reads the data from the next address and outputs it, until the MCU disables SPI chip selection;

⑥ MCU disables the SPI chip selection of CH374 to end the current SPI operation.

The figure below is an SPI logic sequence diagram. The first one writes 34H to 12H addresses, and the

second one reads 78H from 56H address.



6.4. Other Hardware

Any pins of CH374 not used in the actual circuit can be suspended.

ACT# pin of CH374 is used for the status indication. In USB device mode, BIT_SETP_LED_ACT selects to activate the event that ACT# pin outputs the low level, USB transceiving transmission process related to itself by default, or selects all transmissions of USB host, including SOF package. In the USB host mode, when the USB device is disconnected, the pin outputs a high level; when the USB device is connected, the pin outputs a low level. ACT# pin of CH374 can be externally connected to an LED with a current limiting resistor connected in series to indicate the relevant status.

UD+ and UD- pins of CH374 are USB signal lines, which should be directly connected to the USB bus when working in USB device mode; yet they can be directly connected to USB device when working in USB host mode. If a fuse resistor or inductor or ESD protection device is connected in series for chip safety, the AC and DC equivalent series resistors should be within 5Ω.

UEN pin of CH374 is used to control the output enable of UD+ and UD- USB signal lines. For CH374T chip without UEN pin, BIT_CTRL_OE_POLAR must be set to 1; for CH374S chip that UEN pin can control whether the USB signal output is allowed, UEN pin can be connected to the power line of the USB device after being connected with a 2KΩ resistor in series, so as to avoid the USB device to send USB signals when losing its operating power supply. UEN changes from invalid to valid, and can also be used to wake up CH374 in sleep state.

CH374 has a built-in power on reset circuit. Generally, no external reset is required. RSTI pin is used to input an asynchronous reset signal from the outside; when RSTI pin is at high level, CH374 will be reset; when RSTI pin recovers to a low level, CH374 will continuously delay reset for about 25mS, and then enter the normal working status. In order to reliably reset and reduce external interference during the power-on period, a capacitor with a capacity of about 0.1uF can be connected across the RSTI pin and VCC. RST pin and RST# pin are reset status output pins, which are respectively active at high level and active at low level; RST pin and RST# pin output high level and low level respectively when CH374 is powered on or externally forced to be reset, or during reset delay, and when the watchdog timer overflows after the watchdog is enabled. After CH374 internal reset is complete, RST pin and RST# pin will continue to delay for tens of milliseconds and then restore to low level and high level respectively. RST and RST# pins are used to provide power on reset signals to the external MCU. Any write operation on CH374 can clear the watchdog timer.

CH374F chip supports both external clock mode and internal clock mode, and other CH374s only support external clock mode.

When CH374 works normally in the external clock mode, 24MHz clock signal shall be provided for it

externally. Generally, the clock signal is generated by the built-in inverter of CH374 through the crystal stable frequency oscillator. The peripheral circuit is only required to be connected with a crystal with a nominal frequency of 24MHz between XI and XO pins, and connected with a high frequency oscillating capacitor to the ground for XI and XO pins respectively. If the 24MHz clock signal is inputted directly from the outside, it shall be inputted from the XI pin, and the XO pin is suspended.

In the internal clock mode of CH374F chip, XI pin shall be connected to GND and XO pin shall be suspended, so as to save the external crystal and oscillating capacitor. The accuracy of the built-in clock does not meet the USB specification. It is not recommended for USB host and may not be applicable to some USB devices.

SLP pin of CH374 is the sleep state output, and outputs low level by default. If BIT_CTRL_OSCIL_OFF is set to 1 and the clock oscillator is turned off, CH374 will go to sleep and SLP pin will output the high level and restore low level until CH374 wakes up.

CKO pin of CH374 is a programmable clock output, which is used to provide 3MHz to 24MHz clock signal for MCU. It supports the dynamic adjustment of clock frequency and can smoothly transit. The pin will stop the clock output after CH374 sleeps.

CH374 supports supply voltage of 5V or 3.3V (chips with batch number of 2032XXXXX only support 5V voltage). When a 5V operating voltage is used, VCC pin of CH374 will input an external 5V power supply, and the V3 pin shall be connected to an external power decoupling capacitor with a capacity of about 0.01uF to 0.1uF. When 3.3V operating voltage is used, V3 pin of CH374 shall be connected to VCC pin, and an external 3.3V power supply shall be inputted at the same time, and the operating voltage of other circuits connected to CH374 shall not exceed 3.3V. It is recommended to set the register bit BIT_CTRL_USB_POWER to 1 and turn off the power regulator to save power (from several uA to several uA, the sleeping current is saved by 80%).

6.5. Internal Structure

In function, CH374 is basically a pure interface chip after the command interpreter, the control transmission protocol processor and the universal firmware program are removed from CH375 chip. Because the protocol processor and the firmware program are removed, the external MCU program is more complex. However, internal processing and other intermediate links are reduced, so the speed of the interface with MCU is improved.

CH374 has a USB host mode and USB device mode integrated master-slave USB interface engine SIE and a root-hub, which are used for completion of physical USB data receiving and sending, automatic processing of bit tracking and synchronization, NRZI encoding and decoding, bit stuffing, conversion between parallel data and serial data, CRC data check, transaction handshake, error retry and USB bus status detection, etc.

There are 7 physical endpoints inside CH374:

- Endpoint 0 is the default endpoint and supports upload and download. The size of upload and download buffers is respectively 8 bytes.
- Endpoint 1 includes the upload endpoint and the download endpoint. The size of upload and download buffers is respectively 8 bytes. The number of the upload endpoint is 81H and the number of the download endpoint is 01H;
- Endpoint 2 includes the upload endpoint and the download endpoint. The size of upload and download buffers is respectively 64 bytes. The number of the upload endpoint is 82H and the number of the download endpoint is 02H.
- The host endpoint includes the output endpoint and the input endpoint. The size of output and input buffers is respectively 64 bytes, and the host endpoint and the endpoint 2 share the same set of buffers. The send buffer of the host endpoint is the upload buffer of the endpoint 2, and the receive buffer of the host endpoint is the download buffer of the endpoint 2 and can be extended to 128 bytes.

Endpoints 0, 1, and 2 of CH374 are only used in USB device mode, and only host endpoints are used in

USB host mode. In USB host mode, CH374 supports a variety of commonly used USB low-speed devices, full-speed devices and USB devices cascaded through USB-HUB. The endpoint number of USB devices can be 0 to 15, up to 31 endpoints can be supported in both directions, and the packet length of USB devices can be 0-64 bytes. The maximum packet length in the receiving direction can be 0 to 128 bytes.

6.6. Operation Procedure for ROOT-HUB

CH374 has a 3-port ROOT-HUB. ROOT-HUB is only used in USB host mode, and only UD+ and UD- of HUB0 can be used for USB transmission in USB device mode. The usage of ROOT-HUB is as follows:

① Set BIT_SETP_HOST_MODE to enable the USB host mode. Set BIT_SETP_AUTO_SOF to allow CH374 to automatically generate SOF packets, and clear BIT_HUB_DISABLE to allow ROOT-HUB.

② Wait for the USB device to be plugged. BIT_IF_DEV_DETECT is 1, indicating that USB device plugging is detected.

③ Inquire BIT_HUB0_ATTACH, BIT_HUB1_ATTACH and BIT_HUB2_ATTACH, analyze which HUB port has a USB device plugging event. The plugging event will automatically clear BIT_HUB?_EN of corresponding HUB port (? represents 0/1/2, the same below).

④ If a new USB device is plugged, a full-speed or low-speed USB device can be distinguished by inquiring BIT_IF_USB_DX_IN, BIT_HUB1_DX_IN and BIT_HUB2_DX_IN. For a low-speed USB device, set the corresponding BIT_HUB?_POLAR.

⑤ Reset the USB bus for the corresponding HUB port by setting BIT_HUB?_RESET.

⑥ Wait for the USB device to be connected by inquiring BIT_HUB?_ATTACH after USB bus reset is completed.

⑦ Once the USB device is connected, enable the USB port by setting BIT_HUB?_EN, and delay by tens of mS until the device is stable.

⑧ Initialize the enumeration of USB device at 0# address according to the standard procedure, and assign a non-conflicting USB address. If initialization fails and still fails after retry, and the USB device must be aborted, BIT_HUB?_EN must be cleared to close the corresponding HUB port and avoid interference with other USB devices.

⑨ In the initial enumeration process and the subsequent normal communication process, if the target device is a low-speed USB device, BIT_SETP_LOW_SPEED must be set to select low-speed transmission before USB transmission operation, and the bit shall be cleared after transmission. If the target device indirectly operates a low-speed USB device through an external HUB, set BIT_SETP_LOW_SPEED to select low speed, and set BIT_HUB_PRE_PID to enable the low-speed refix packet PRE PID, and then clear the two bits after transmission.

⑩ MCU software must establish an information record for each HUB port, including whether USB device exists, whether it is low-speed or full-speed, whether USB address has been assigned and what the USB address is, whether USB configuration is completed, function or type of USB device, set of endpoint numbers and attribute of each endpoint, maximum packet length and so on. The corresponding information record must be updated in time after USB device plugging is detected. Before the USB device is operated each time, set BIT_SETP_LOW_SPEED according to the destination or port record, and set REG_USB_ADDR, select the endpoint number and PID. For low-speed USB devices connected through external HUB, set BIT_HUB_PRE_PID PRE PID to enable the low-speed prefix packet PRE PID, and then perform the USB transmission of the specified endpoint, and clear BIT_SETP_LOW_SPEED and BIT_HUB_PRE_PID after transmission.

⑪ Based on the above operation, determine the state of the USB device according to the following rules. If BIT_HUB?_ATTACH is 0, there will be no USB device connected on this port. If BIT_HUB? _ATTACH is 1 and BIT_HUB? If _EN is 0, the USB device of this port has just been connected and not been initialized (or reconnected after being disconnected). If BIT_HUB? _ATTACH is 1 and BIT_HUB?_EN is 1, the USB device of this port has been successfully initialized.

7. Parameters

7.1. Absolute Maximum Value

Critical value or exceeding the absolute maximum value may cause the chip to work abnormally or even be damaged.

Name	Parameter description		Min.	Max.	Unit
TA	Operating Ambient temperature	VCC=5V or VCC=V3=3.3V, external clock	-40	85	°C
		VCC=V3=3.0V, external clock	-40	70	
		VCC=5V or VCC=V3=3.3V, internal clock	-20	70	
TS	Ambient temperature during storage		-55	125	°C
VCC	Supply voltage (VCC connects to power, GND to ground)		-0.5	6.0	V
VIO	Voltage on the input or output pins		-0.5	VCC+0.5	V

7.2. Electrical Parameters

Test conditions: TA=25°C, VCC=5V, excluding the pins connected to the USB bus.

If the supply voltage is 3.3V, all current parameters in the table need to be multiplied by a factor of 40%.

Name	Parameter description		Min.	Typ.	Max.	Unit
VCC	Power supply voltage	V3 pin is not connected to VCC pin	4.4	5	5.3	V
		V3 pin connected to VCC pin	3.0	3.3	3.6	
ICC	Total supply current during operation	VCC=5V		5	25	mA
		VCC=3.3V		2	12	
ISLP	Supply current at the low power consumption status I/O pin suspended/ internal pull-up	VCC=5V		0.07	0.15	mA
		VCC=3.3V		0.06	0.09	
		VCC=3.3V Turn off the regulator		0.003	0.01	
VIL	Low level input voltage		0		0.7	V
VIH	High level input voltage		2.0		VCC	V
VOL	Low level output voltage (4mA draw current)				0.5	V
VOH	High level output voltage (4mA output current)		VCC-0.5			V
IUINT	High-level pull-up output current of INT# pin		30	280	360	uA
IUACT	High-level pull-up output current of ACT# pin		60	300	800	uA
IUP	Input current at the input terminal of other built-in pull-up resistor		3	150	250	uA
IDUEN	UEN pin input current of built-in pull-down resistor		-40	-100	-350	uA
IDRI	RSTI pin input current of built-in pull-down resistor		-60	-100	-210	uA
VR	Voltage threshold of power-on reset		2.1	2.5	3.0	V

7.3. Basic Timing

Test conditions: TA=25°C, VCC=5V or VCC=3.3V.

Name	Parameter description	Min.	Typ.	Max.	Unit
FCLK	Input clock frequency of XI pin in USB host mode	23.99	24.00	24.01	MHz
FCLKI	Internal clock frequency in CH374F built-in clock mode	23.52	24.00	24.48	MHz
TPR	Internal reset time of power-on	13	25	40	mS
TRI	Effective signal width of external reset input	100			nS
TRD	Reset delay after external reset input	14	17	20	mS
TRO	Output reset time of power on RST and RST# pins	60		150	mS
TDGC	Watch dog timing cycle (overflow time)	950		1200	mS
TDGR	Reset time generated by watchdog timing overflow	60	64	140	mS
TWAK	Chip wake-up completion time	3	5	15	mS
TINT	Interrupt pulse width of INT# pin in low level pulse mode	7		16	mS

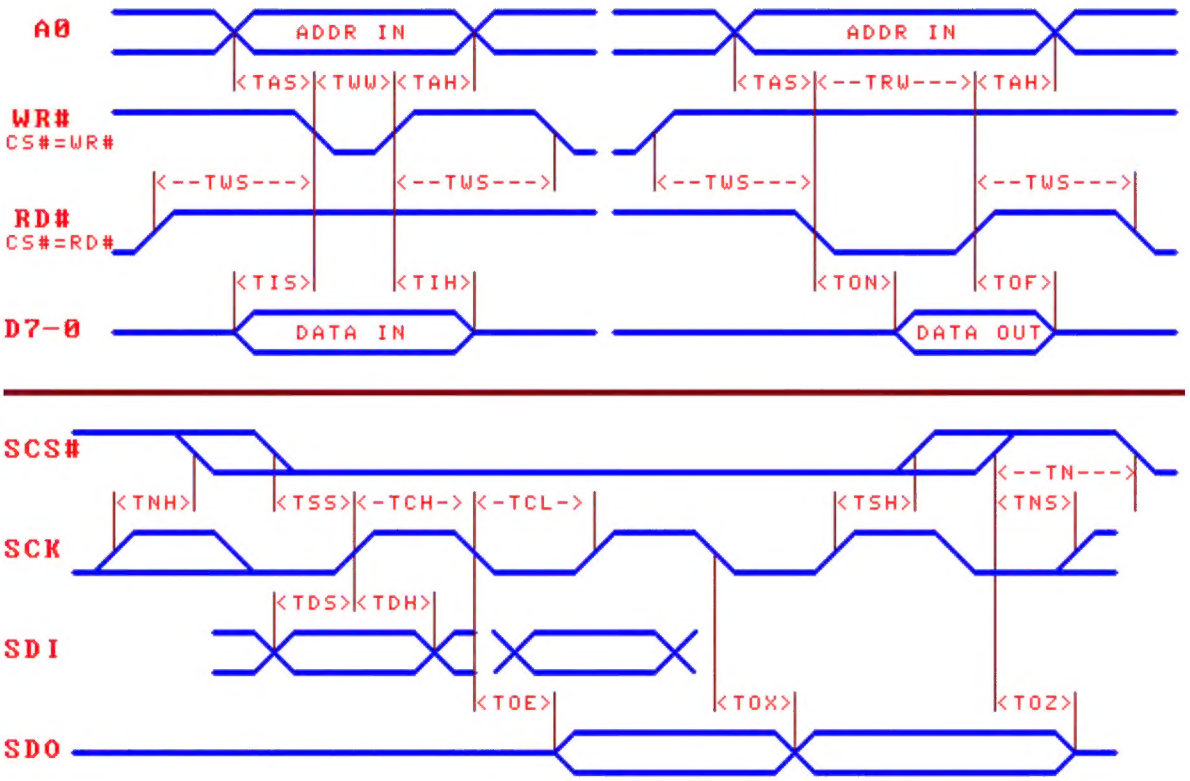
7.4. Parallel Timing

Test conditions: TA=25°C, VCC=5V, the parameter in brackets VCC=3.3V, referring to the attached drawing below.

(RD means that the RD# signal is valid and the CS# signal is valid; WR#=1& RD#=CS#=0 performing a reading operation)

(WR means WR# signal is valid and CS# signal is valid, WR#=CS#=0 performing a writing operation)

Name	Parameter description	Min.	Typ.	Max.	Unit
TWW	Width of effective strobe writing pulse WR	30 (45)			nS
TRW	Width of effective strobe reading pulse RD	30 (45)			nS
TWS	Interval width of strobe reading or strobe writing pulse	120 (140)			nS
TAS	Address input setup time before RD or WR	4 (6)			nS
TAH	Address input maintaining time after RD or WR	4			nS
TIS	Data input setup time before write strobe WR	1			nS
TIH	Data input maintaining time after strobe writing WR	4 (6)			nS
TON	Effective strobe reading RD to effective data output		18 (25)	25 (40)	nS
TOF	Ineffective strobe reading RD to ineffective data output			18 (25)	nS



7.5. SPI Serial Timing

Test conditions: TA=25°C, VCC=5V, the parameter in brackets VCC=3.3V, referring to the attached drawing above.

Name	Parameter description	Min.	Typ.	Max.	Unit
TSS	Effective setup time of SCS# before SCK rising edge	20 (30)			nS
TSH	Effective maintaining time of SCS# after SCK rising edge	20 (30)			nS
TNS	Ineffective setup time of SCS# before SCK rising edge	20 (30)			nS
TNH	Ineffective maintaining time of SCS# after SCK rising edge	20 (30)			nS
TN	Ineffective time of SCS# (SPI operation interval time)	80 (120)			nS
TCH	SCK clock high-level time	14 (18)			nS
TCL	SCK clock low-level time	18 (24)			nS
TDS	SDI input setup time before SCK rising edge	4 (6)			nS
TDH	SDI input maintaining time after SCK rising edge	3			nS
TOE	Effective output from SCK falling edge to SDO	2	12 (18)	18 (25)	nS
TOX	Output change from SCK falling edge to SDO		8 (12)	12 (18)	nS
TOZ	Ineffective SCS# to ineffective SDO output			18 (25)	nS

8. Application

8.1. Parallel Port Mode

This is the paralel port connection circuit of CH374. The VCC power supply of CH374 in the figure is 5V.

Capacitor C3 is used for decoupling the internal power node of CH374. C3 is a monolithic or high-frequency ceramic capacitor with a capacity of 0.01μF to 0.1μF. Capacitor C4 is used for decoupling the external power source, and C4 is a monolithic or high-frequency ceramic capacitor with a capacity of 0.1μF.

Crystal X1 and capacitors C1 and C2 are used in the clock oscillation circuit of CH374. The USB-HOST mode requires accurate clock frequency, and the frequency of X1 is 24MHz±0.4‰. Refer to the settings in the manual. The frequency of X1 can also be 12MHz. C1 and C2 are monolithic or high-frequency ceramic capacitors with a capacity of about 22pF. The capacitor C5 is optional and only used to extend the reset time of CH374 when the power supply is turned on. C5 can be omitted in the general application circuits, or CH374 reset can also be controlled by the common I/O pin of MCU.

If CH374F finished board uses the built-in clock mode, only remove X1 and C1, and replace C2 with a 0Ω resistor.

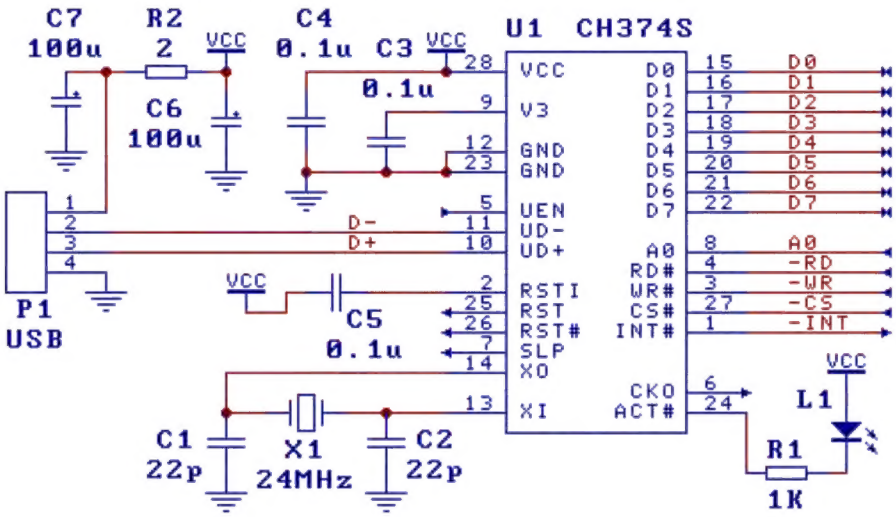
It is recommended that the decoupling capacitors C3 and C4 shall be as close as possible to the connected pins of CH374 when the printed circuit board PCB is designed; the D+ and D- signal lines shall be close to parallel wiring, and ground wire or covered copper shall be provided on both sides to reduce the external signal interference; the length of the signal lines related to the XI and XO pins shall be shortened as far as possible to reduce the external interference of the high-frequency clock. The ground wire or covered copper shall surround the relevant components.

The resistor R2 and the capacitor C7 are generally used to limit the peak current in the USB-HOST application when the USB device is just connected, and the resistor R2 can be replaced by a current limiting resistor or inductor. UEN pin can be connected to the USB power supply through a 2KΩ resistor to turn off the USB signal output when the USB device loses the working power supply. LED L1 and the current limiting resistor R1 are optional and used for status indication.

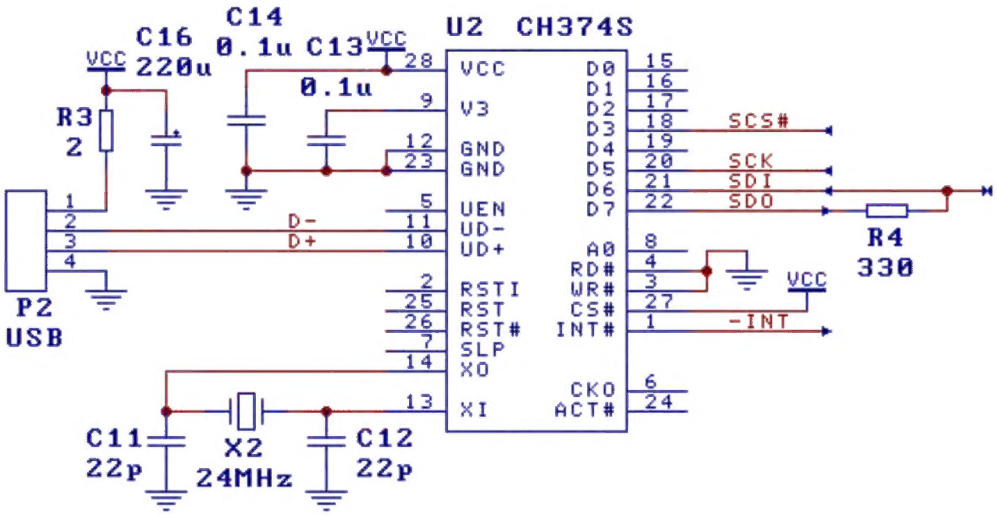
CH374 also provides the following auxiliary signals for MCU system: RST and RST# pins can be used to provide MCU with power on reset and watchdog reset signals; CKO pin can be used to provide the frequency dynamic programming clock signal for MCU; SLP pins can be used to provide automatic wake-up control for MCU or other peripherals after power-off in sleep mode.

If the interrupt request output pin INT# is not connected, MCU program can also be replaced by querying the interrupt flag register.

CH374 has a general-purpose passive parallel interface, which can be directly connected to a variety of DSPs, MCUs, and CPUs through D0-D7, A0, -RD, -WR, -CS and -INT signals.



8.2. SPI Serial Port Mode



If RD# and WR# pins of CH374 are at the low level (grounded) and the CS# pin is at the high level (connected to a positive power source), then CH374 will work in SPI serial mode. In the SPI serial port mode, CH374 only needs to be connected to 5 signal lines with DSP/MCU: SCS# pin, SCK pin, SDI pin, SDO pin, and INT# pin. Other pins can be suspended.

To save pins, the INT# pin can be left unconnected, and the interrupt flag register can be queried instead, but the query efficiency is low.

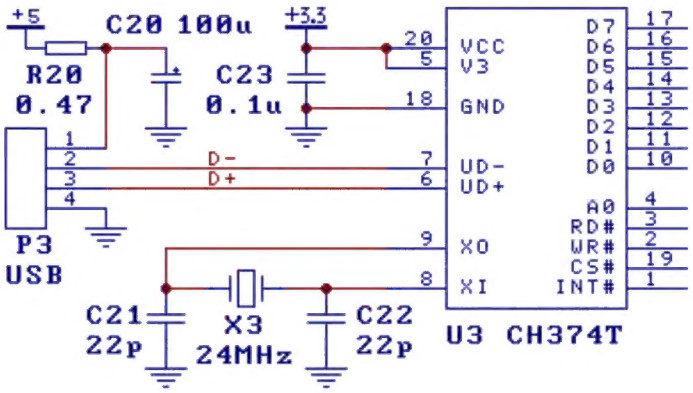
In order to save pins, SDO output pin of CH374 can be connected to a 330Ω resistor R4 in series and then connected to SDI pin in parallel, and then connected with SDI and SDO of MCU. Of course, SDO pin of MCU must be three-state output, or output can be turned off.

Other peripheral circuits are basically the same as that in the parallel port mode except that the connections in the SPI serial port mode are fewer than that in the parallel port mode. In terms of software programming, all functional programs are basically the same, except for the interface subroutines at the hardware abstraction layer.

The SPI serial port mode of CH374 provides a low-cost interface mode for USB communication and control of USB devices for the limited MCU of I/O pins or MCU without parallel bus.

8.3. Operating Voltage 3.3V

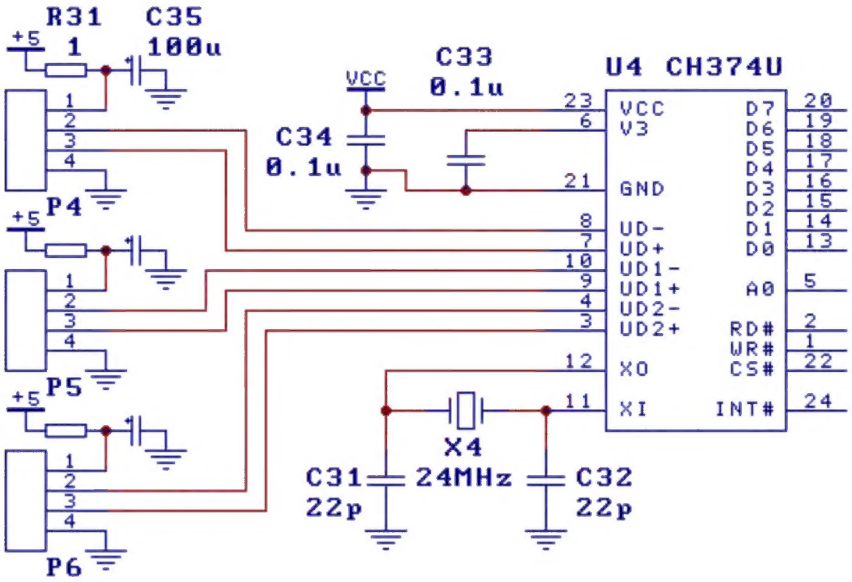
VCC of CH374 in the figure is 3.3V or 3V, so V3 pin must be short-circuited with VCC to input 3.3V together. However, as the USB supply voltage of the USB host terminal, the voltage supplied to USB port P3 must still be 5V.



8.4. Three Devices Connected by Built-in HUB

CH374F and CH374U chips have 3-port Root-HUB. When being used as USB-Host, they can be

connected to 3 USB devices at the same time, supporting mixed applications of USB full-speed and low-speed devices. Ports P5 and P6 can only be used to connect external USB devices in Host mode, and port P4 can be used to connect external USB devices in Host mode and connect external Host in Device mode.



8.5. ROOT-HUB Example Program

Refer to CH374 evaluation board data CH374EVT\EXAM\EMB_HUB\ROOTHUB.C program, support three ports of built-in ROOT-HUB, and also support external secondary HUB cascade to directly or indirectly operate the full-speed or low-speed USB devices.

Refer to EXAM14 in CH374LIB, support built-in ROOT-HUB, three ports are respectively used for reading and writing USB flash disk files, and controlling USB keyboard or mouse, etc.

Refer to EXAM15 in CH374LIB, and achieve file replication between two USB flash disks through two ports of ROOT-HUB.